UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/285,899	04/08/1999	SHUNPEI YAMAZAKI	0756-1950	4276

31780 7590 09/08/2004

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
TON, MINH TOAN T	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/285,899	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Toan Ton	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6-09-04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 9-16,21-24,33-36,50-52,54 and 57-97 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9-16, 21-24, 33-36, 50-52, 54 and 57-97 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. Claims 9-16, 21-24, 33-36, 50-52, 54 and 57-97 rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba (US 5227900) in view of Takeshita (JP 61-141174) and Wakai et al (US 5055899).

Wakai discloses (see figures 1-2) that an active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68). Wakai solves the short-circuiting problem by forming the insulation layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer. Therefore, it would have been obvious to one of ordinary skill in the art to employ an insulating layer having a contact hole and formed between the pixel electrode and the drain electrode for avoiding disadvantages including short-circuiting.

See other detailed explanations in the office action mailed 06-05-01.

The use of antiferroelectric liquid crystal would have been at least an obvious variation (alternative, not patentably distinct) to the use ferroelectric liquid crystal. Both offer similar advantages such as memory effect, high-speed response. Therefore, it would have been at least obvious to employ either ferroelectric LC or antiferroelectric LC (alternative, not patentably distinct) for similar advantages such as memory effect, high-speed response.

Response to Arguments

2. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Takeshita teaches that the use of leveling film of organic resin over the TFT is common (an usual way) in the art. Further, Wakai discloses (see figures 1-2) that an active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68). Wakai solves the short-circuiting problem by forming the insulation layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer. Therefore, it would have been obvious to one of ordinary skill in the art to employ an insulating layer (organic resin) having a contact hole and formed between the pixel electrode and the drain electrode for avoiding disadvantages including short-circuiting.

Contact Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Ton whose telephone number is (571) 272-2303.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 2, 2004

TOAN TON
PRIMARY EXAMINER